REMARKS

Claims 1-35 all the claims pending in the application. Claims 1, 2, 4-35 stand rejected upon informalities. Claims 1, 2 and 4-23 stand rejected on prior art grounds. In addition, the drawings are objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

1. Rule 83 Drawing Objection

The Office Action objects to the setup and hold tests defined by claims 5, 6, 10, 13, 26, and 32 as not being shown in the drawings. However, Applicants note that the difference between projected and measured setup is shown in Figure 11 and the computer system shown in Figure 7 performs the setup and hold tests described in the specification.

Further, since setup and hold tests are requirements on the separation of two edges (or types of signals in the language of the specification and claims), they are difficult to depict. The actual separation of two edges (which is compared against a setup or hold test requirement) can be depicted, and such a separation between a gating signal edge and a subsequent clock edge is depicted in Figure 6B (element 605) and described in paragraph 0045. This separation is shown to be between the modified sensing points according to the invention, and therefore depicts the setup test as well.

The opposite separation, between a clock edge and a subsequent gating signal edge, which would be compared against a hold test is similar. The symmetry between the hold test and the setup test separation would be easily understood by one of ordinary skill in the art. Specifically, in paragraph 0054 it is explained that the modification of tests can be applied in any case in which a static timing analysis test is used to ensure that a first transition on one input of a circuit prevents the propagation of second transition on another input of the circuit," A hold test is just such a case, where the first transition is of a clock signal and the second transition is of a gating signal, and this is explained in paragraph 0016.

Therefore, Applicants respectfully submit that the features defined by claims 5, 6, 10, 13, 26, and 32 are properly illustrated in the drawings and the Examiner is respectfully requested to reconsider and withdraw this objection.

II. The 35 U.S.C. §112, First Paragraph, Rejection

Claims 1, 2 and 4-35 stand rejected under 35 U.S.C. §112, first paragraph. Referring to the paragraph numbers in the Office Action, Applicants respond as follows.

With respect to paragraph 4a, the output is implicitly depicted in the clock waveform of both figures. Specifically, the solid portions of the clock waveform in each of these figures are the output signal. The portions of the dashed waveforms which remain low represent the value of the output which could occur if the gate signal were low during these intervals. The portions of the dashed waveforms which go high represent the value of the input clock during intervals in which it is blocked from propagating to the output by the gate signal. In paragraph 0005, the specific operation of this circuit is explained, which will further aid in the understanding of Figures 2-3: "As an example, an AND gate 140 used for clock gating is shown in FIG. 1 along with idealized clock and gate signal waveforms, which are shown in FIG.2. In FIG. 1, the AND gate 140 outputs 120 a high signal only when the clock 100 and gate 110 signals are also at a high state. Therefore, the output 120 would have a high signal only when both the gate 110 and clock signal 100 are high during time 200. Conversely, the output 120 would be low during the time 201 when only the clock signal was high. In this example, the gate signal 110 prevents the clock signal 100 from being output 120 during time 201. This is commonly referred to as "clock gating"."

With respect to paragraph 4b, the concepts of setup and hold tests in static timing analysis are very well known. In paragraph 0009 the concept of propagated clock gating tests is explained as a comparison between two ATs (arrival times), thus it will be easily understood that "AT test" in paragraph 0052 means a setup or hold test. Once again, tests are relationships between two signals, and therefore are not amenable to direct illustration.

With respect to paragraph 4c, computation of arrival times (ATs) and slews are well-known in the prior art of static timing analysis. The clock and gate subscripts or suffixes on these merely indicate the signals whose ATs and slews are being computed.

With respect to item 4e in the Office Action, the specific identity of the signal attached to the lower input of the AND gate in Figure 8 was not described in the specification because it was not needed for illustrative purposes of the figure, which is to demonstrate that larger capacitive loading of a gate output increases delay when a transition on the output occurs due to an input transition, but does not increase the time required for input transitioning to the controlling state for a gate (e.g., zero for an AND gate) so as to prevent a transition on the output due to a subsequent transition on another input. In the context of the specification, which refers to clock gating, Applicants submit that it would be clear to one ordinary skill in the art that the upper input and the AND gate in Figure 8 is a clock input and that the lower input is a gating input.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 1, 2, 5, 11-13, 17-19, 24, 26, 30 and 32 stand rejected under 35 U.S.C. §112, second paragraph. Applicants respond as follows.

Figures 2, 3, 5, 6A, and 6B were previously corrected; however, those corrections do not appear to have been considered prior to drafting the Office Action. These drawing corrections more clearly illustrate the first-type signal that enables output and the second-type signal that inhibits output. These proposed drawing corrections do not add new matter because paragraph 0005 explains that the high gate signal enables output and the low gate signal inhibits output (see the bottom of page 3 and top of page 4 of the specification). Applicants respectfully submit that with these corrections, the reader can clearly see that the invention does not alter the sensing of the output inhibiting signal (second-type of signal) but instead only changes the sensing of the output enabling signal (first-type of signal) as shown in Figure 6B. Therefore, once again, Applicants submit that the independent claims are clear and fully supported by the specification.

With respect to claims 5 and 6, Applicants again note that the difference between projected and measured setup is shown in Figure 11 and the computer system shown in Figure 7 performs the setup and hold tests described in the specification.

Further, since setup and hold tests are requirements on the separation of two edges (or types of signals in the language of the specification and claims), they are difficult to depict. The actual separation of two edges (which is compared against a setup or hold test requirement) can be depicted, and such a separation between a gating signal edge and a subsequent clock edge is depicted in figure 6B (element 605) and described in paragraph 0045. This separation is shown to be between the modified sensing points according to the invention, and therefore depicts the setup test as well.

The opposite separation, between a clock edge and a subsequent gating signal edge, which would be compared against a hold test is similar. The symmetry between the hold test and the setup test separation would be easily understood by one of ordinary skill in the art. Specifically, in paragraph 0054 it is explained that the modification of tests can be applied in any case in which a static timing analysis test is used to ensure that a first transition on one input of a circuit prevents the propagation of second transition on another input of the circuit," A hold test is just such a case, where the first transition is of a clock signal and the second transition is of a gating signal, and this is explained in paragraph 0016.

The "means" for computing setup and hold tests is the computer system of Figure 7. The formulae which are computed using those means are given in the specification:
In paragraph 0050: "$Slew_{clock}$ * 0.625 - $delay_{clock}$- $Slew_{gate,}$ * K + $delay_{gate}$ ",
In paragraph 0052: "In another embodiment, the invention uses the least pessimistic of the input-to-input and "propagated" AT tests for the disabling setup test and the enabling hold test." The propagated AT tests were explained earlier in paragraph 0009, and input-to-input tests will be easily understood from the discussion in paragraph 0008 to be a direct comparison between AT_{clock} and $AT_{gate,}$ thus giving a setup test value of zero), and (In paragraph 0042) 8 and 108.

Therefore, Applicants submit that the claims are definite and particularly define the subject matter which Applicants regard as the invention. Thus, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. The Prior Art Rejections

Claims 1, 2 and 4-23 stand rejected under 35 U.S.C. §102(a) as being anticipated by Wu (US Patent 6,167,001). Applicants respectfully traverse this rejections based on the following discussion. The Wu patent cited refers to a method for making hardware measurements, and specifically refers to successively changing the separation between two signals until an error is detected. This is very different from the claimed invention, which is an analysis method typically applied before any hardware has been built. The claims should be understood in the context of the specification, in which signals timings (ATs, slews) clearly refer to values computed in static timing analysis, and not to hardware measurements. Therefore "modifying the timing of a sensing" of a signal must be understood not to be a change in the application of a signal to hardware, as in Wu, but to be a change in the way a timing value is computed in static timing analysis. In contrast, in Wu the modification is in the actual arrival times of the signals at the flip-flop and not in the way those arrival times are sensed (they are always sensed by determining whether or not a flip-flop stores the expected value). This change in arrival times is accomplished by delay setting circuitry 32a of Figure 14, and resulting in different physical signals arriving at the flip-flop being tested.

Thus, Wu is really directed to a process of successively changing the separation between signals until an error is detected in order to test the outer operating parameters of a given device. To the contrary, the claimed invention relates to sensing the enabling gating signal at an earlier point in time in order to reduce pessimism and permit more aggressive designs to test successfully.

More specifically, the abstract of Wu explains that the processing in Wu involves testing devices by repeatedly applying different pulses at progressive intervals until an error is detected. This finds, for example, the minimum signal delay under which the device being tested can properly operate. Wu is silent regarding reducing the slew calculation in order to sense enabling gating signal an earlier point in time, as the claimed invention does. To the contrary, Wu does not alter the way in which signals are sensed, but instead merely alters the timing between different signals.

Therefore, Wu does not teach or suggest the invention defined by independent claims 1, 11, and 17. More specifically, these claims define that the "first-type" signal enables the gating device to output a certain signal (e.g., a clock signal) and that the "second-type" signal inhibits the gating device from outputting such a signal. Then, in the last two lines of independent claims 1, 11, and 17, the invention provides a process of "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed." As explained in paragraph 0045 of the application, this feature of the invention reduces pessimism by reducing the delay calculation within a circuit.

More specifically, the delay savings can be seen when comparing Figures 6A and 6B. Figure 6A shows a fairly pessimistic situation wherein the midpoint 601 in the slew of the gate signal 110 must occur substantially before the midpoint 600 in the slew of the clock signal 100. The difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 is shown as time period 605. To the contrary, as shown in Figure 6B, by utilizing a sensing point that is well in front of the midpoint 600, 601 (utilizing factor K, assuming no load, etc.), the invention is able to reduce the difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 to a much smaller time 606. In other words, the invention is much less pessimistic and utilizes factor K to observe when the gate signal just begins its transition. Then, the invention is able to allow this sense point to occur just before when the clock signal begins its transition, as shown in Figure 6B. In doing so, the invention reduces timing delay requirements dramatically.

Wu does not and cannot teach these features because Wu does not alter when the rising clock signal is sensed. Instead, Wu progressively alters the delay between two separate signals in order to test the operational parameters of various devices. Therefore, Applicants respectfully submit that Wu does not teach or suggest "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed" as defined by independent claims 1, 11, and 17. Thus, independent claims 1, 11, and 17 are not anticipated by Wu. Further, dependent claims 2, 4-10, 12-16, and 18-23 are similarly not anticipated by Wu, not only because they depend from a non-anticipated claimed, but also because of the additional

features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

V. Formal Matters and Conclusion

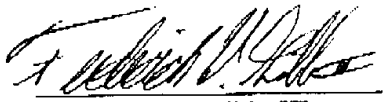
With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. With respect to the objection to the drawings, a Submission of Proposed Drawing Corrections is submitted herewith. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to the claims and drawings.

In view of the foregoing, Applicants submit that claims 1-35, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,



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